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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/752,642	12/29/2000	Peter Lynton Flake	PA1447US	1487
36503	7590 09/27/2005		EXAMINER	
SYNOPSYS, INC.			HARTMAN JR, RONALD D	
c/o A. RICHARD PARK, REG. NO. 41241 PARK, VAUGHAN & FLEMING LLP			ART UNIT	PAPER NUMBER
2820 FIFTH STREET			2121	
DAVIS, CA 95616-2419			DATE MAILED: 09/27/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	09/752,642	FLAKE ET AL.				
Office Action Summary	Examiner	Art Unit				
	Ronald D. Hartman Jr.	2121				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, 'Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim will apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	I. lely filed the mailing date of this communication. C (35 U.S.C. § 133).				
Status						
 1) Responsive to communication(s) filed on 30 Ju 2a) This action is FINAL. 2b) This 3) Since this application is in condition for allowant closed in accordance with the practice under E 	action is non-final. nce except for formal matters, pro					
Disposition of Claims						
4)	vn from consideration. /are rejected.					
Application Papers						
9) The specification is objected to by the Examiner 10) The drawing(s) filed on is/are: a) access Applicant may not request that any objection to the of Replacement drawing sheet(s) including the correction of the original transfer and the correction of the original transfer and the correction of the original transfer and the correction of the co	epted or b) objected to by the Eddrawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	e 37 CFR 1.85(a). ected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:					

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DETAILED ACTION

1. Claims 34-36, 37-38, 40-43, 45-46 and 48-49 are presented for examination.

Response to Arguments

2. Applicant's arguments with respect to claims 34-36, 37-38, 40-43, 45-46 and 48-49 have been considered but are moot in view of the new ground(s) of rejection, as set forth below in this office action.

Claim Interpretations

3. Claim 1, lines 12-13, "the compiled application code" lacks proper antecedent basis. That is, since the applicant has described both the "programming language" and the "hardware description language" to both consist of "code", the examiner has interpreted the claimed "compiled code" to be the collective combination of both, that is, the blending of the languages together.

That being said, it appears that the "wrapper" (claim 34), "the "automatic threading" (claim 34) and the "mapping data types" (claim 35) are all features that essentially used for the same function, that is, to allow communications to occur to and from each different language so that the simulation may utilize more than one programming language. These terms, and the functions associated therewith, appear to correspond to Burgoon's disclosure of an Interpreter (Section 3), which allows for calling, loading and linking. Also See Section 5 and Sections 7.1 and 7.3 for more details.

Claim Objections

4. Claim 1, L 12-13, "the compiled application code" lacks proper antecedent basis.

Claims 40 and 48 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim.

Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. As such, claims

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40 and 48 are rejected in much the same manner as claims 34 and 42, since claims 40 and 48 purportedly do not serve to further limit these claims (34 and 42).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- 6. Claims 34-36, 37-38, 40-43, 45-46 and 48-49 are rejected under 35 U.S.C. 102(a) as being anticipated by "A Mixed-Language Simulator for Concurrent Engineering"; by David A. Burgoon, which was published in March 1998.

As per claims 34 and 42, Burgoon teaches a computer implemented method comprising:

- receiving a description of the digital circuit, wherein a first portion of the description is in a hardware description language and a second portion of the description is in a computer programming language (e.g. Abstract, Section 3 and Section 7);
- blending the first portion and the second portion into an executable simulation, wherein blending the first and second portion involves automatically creating a wrapper for code written in the computer programming language so that code written in the hardware description language can call code written in the computer programming language, and wherein the wrapper facilitates automatic threading, whereby the threading enables the compiled application code to call tasks in the hardware description language (e.g. Abstract and Sections 3 and 7, 7.1, 7.2 and 7.3); and
- executing the executable simulation, wherein executing the simulation allows a designer to simulate operation of the digital circuit (e.g. entire article; pages 16-19).

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As per claims 35 and 43, Burgoon further teaches blending the first and second portions by mapping data types native to the hardware description language to data types native to the computer programming language (e.g. Sections 1, 3 and 7.0, 7.1 and 7.2).

As per claims 37 and 45, Burgoon further teaches the wrapper providing a data communication mechanism between the code written in the HDL and code written in the computer programming language, wherein the data communication mechanism provide mapping between data types in the HDL and the computer programming language (e.g. Sections 1, 3 and 7.0, 7.1 and 7.2).

As per claims 38 and 46, Burgoon further teaches automatically creating the "wrapper" (e.g. inherent to the computer performing the operations necessary for the simulation to occur, wherein the simulation requires communications between two different computer based languages).

As per claims 41 and 49, Burgoon adequately teaches the wrapper outputting a message upon a occurrence pf a call or return, wherein the message can include values associated with the call and return (e.g. calling; Section 3 and Section 7).

Conclusion -

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald D. Hartman Jr. whose telephone number is (571) 272-3684. The examiner can normally be reached on Mon.-Fri., 11:00 - 8:30 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on (571) 272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ronald D Hartman Jr.

Patent Examiner

Art Unit 2121

KROH

September 21, 2005

Anthony Knight Supervisory Patent Examiner

Group 3600